Fig 1 Prior art

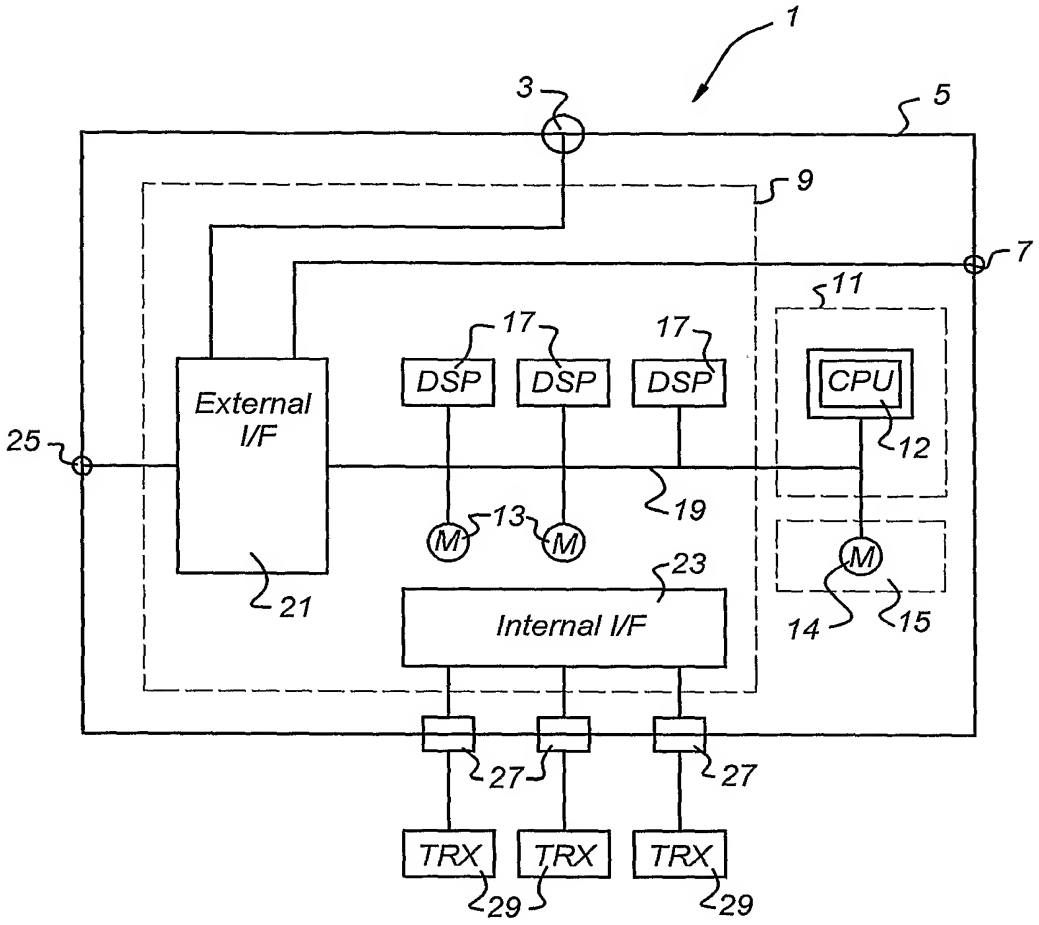


Fig 2

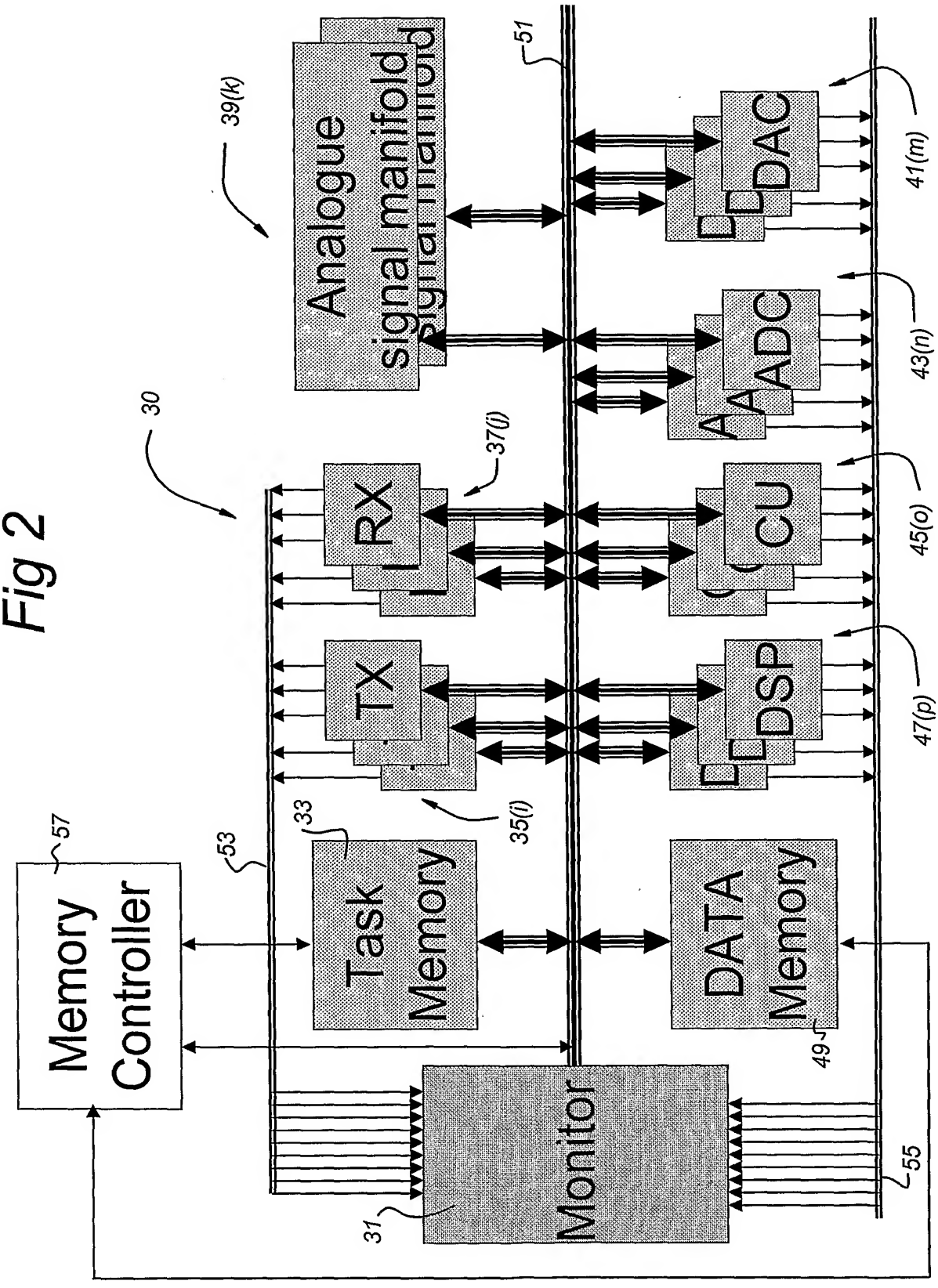

Memory Controller
57
53
Task Memory
33
35(i)
DATA Memory
49
Monitor
31
55
30
RX
37(j)
TX
Analogue signal manifold
39(k)
51
DAC
41(m)
ADC
43(n)
CU
45(o)
DSP
47(p)

Fig 3

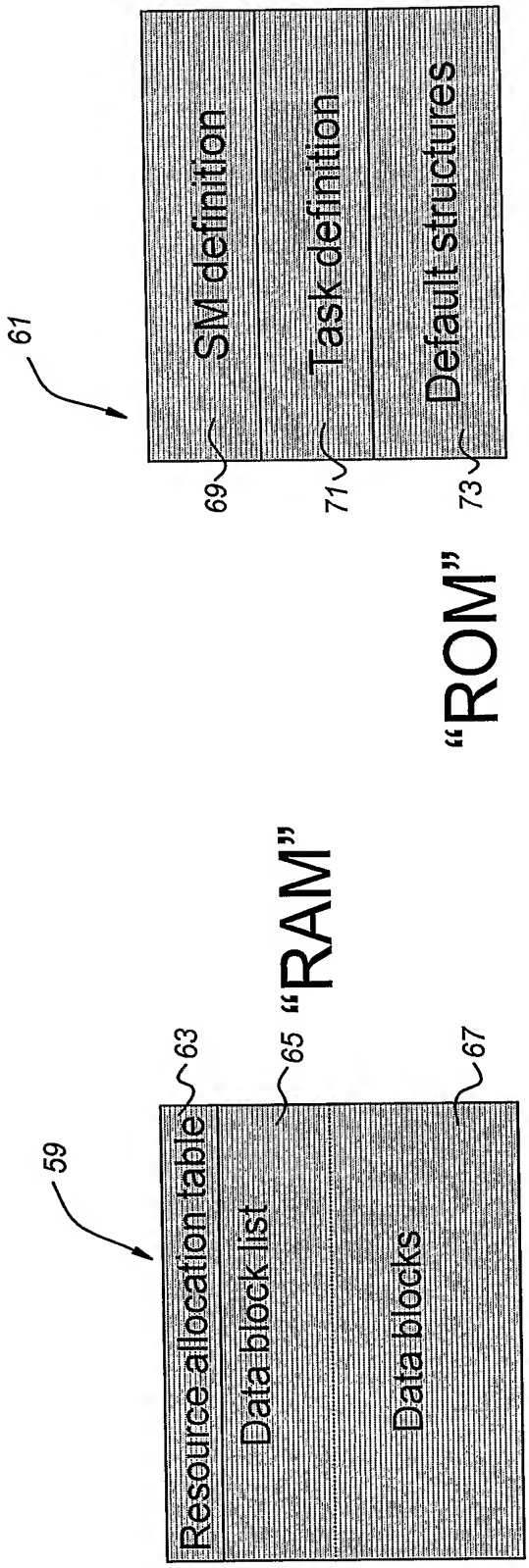

61
SM definition
Task definition
Default structures
69
71
73
"ROM"
"RAM"
59
Resource allocation table
Data block list
Data blocks
63
65
67

Fig 4

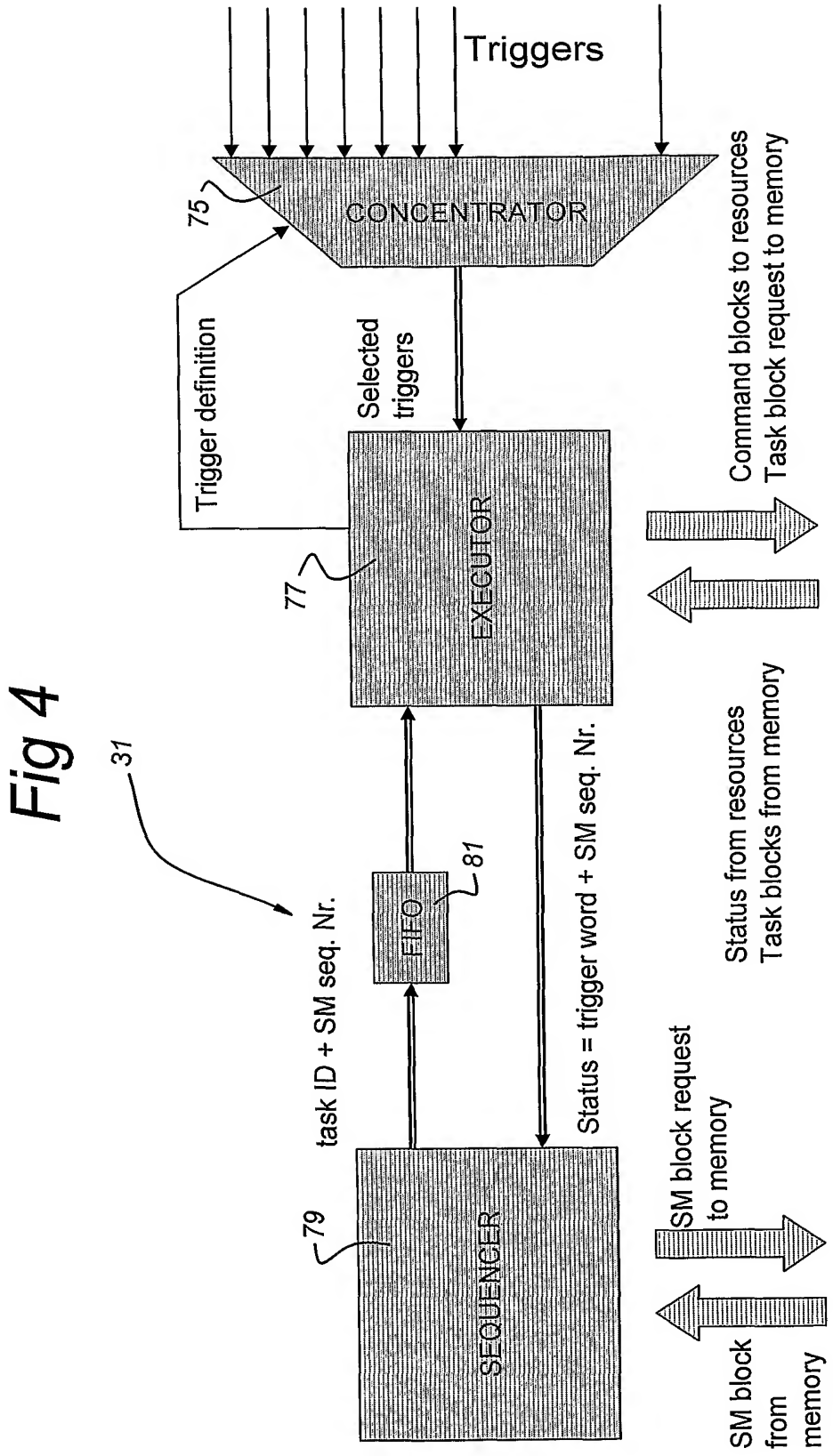

Triggers
75
CONCENTRATOR
Trigger definition
Selected triggers
77
EXECUTOR
Command blocks to resources
Task block request to memory
Status from resources
Task blocks from memory
31
FIFO
81
task ID + SM seq. Nr.
Status = trigger word + SM seq. Nr.
79
SEQUENCER
SM block request to memory
SM block from memory

Fig 5

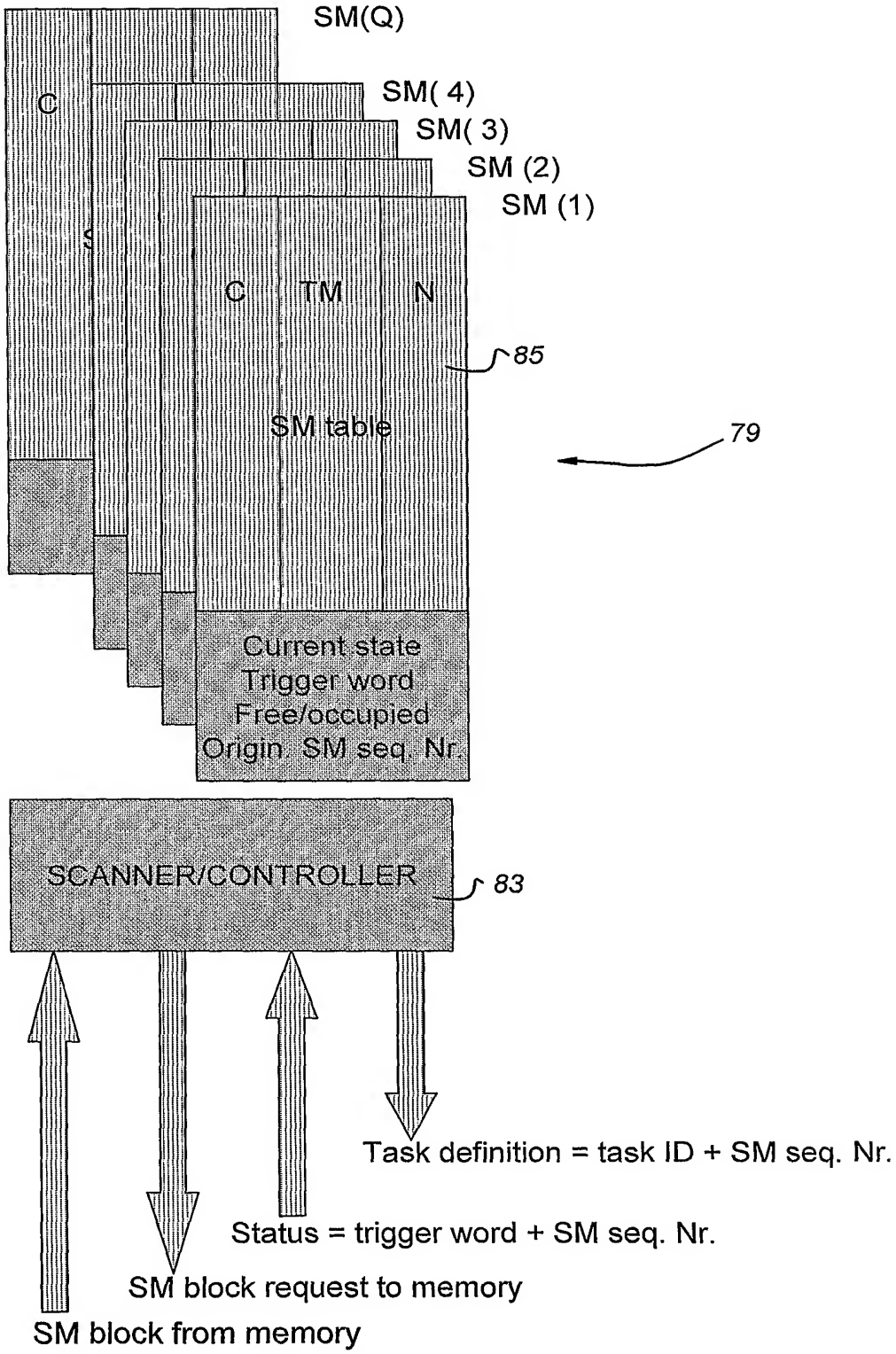

SM(Q)
SM(4)
SM(3)
SM (2)
SM (1)
C
C
TM
N
85
SM table
79
Current state
Trigger word
Free/occupied
Origin SM seq. Nr.
SCANNER/CONTROLLER
83
Task definition = task ID + SM seq. Nr.
Status = trigger word + SM seq. Nr.
SM block request to memory
SM block from memory

Fig 6

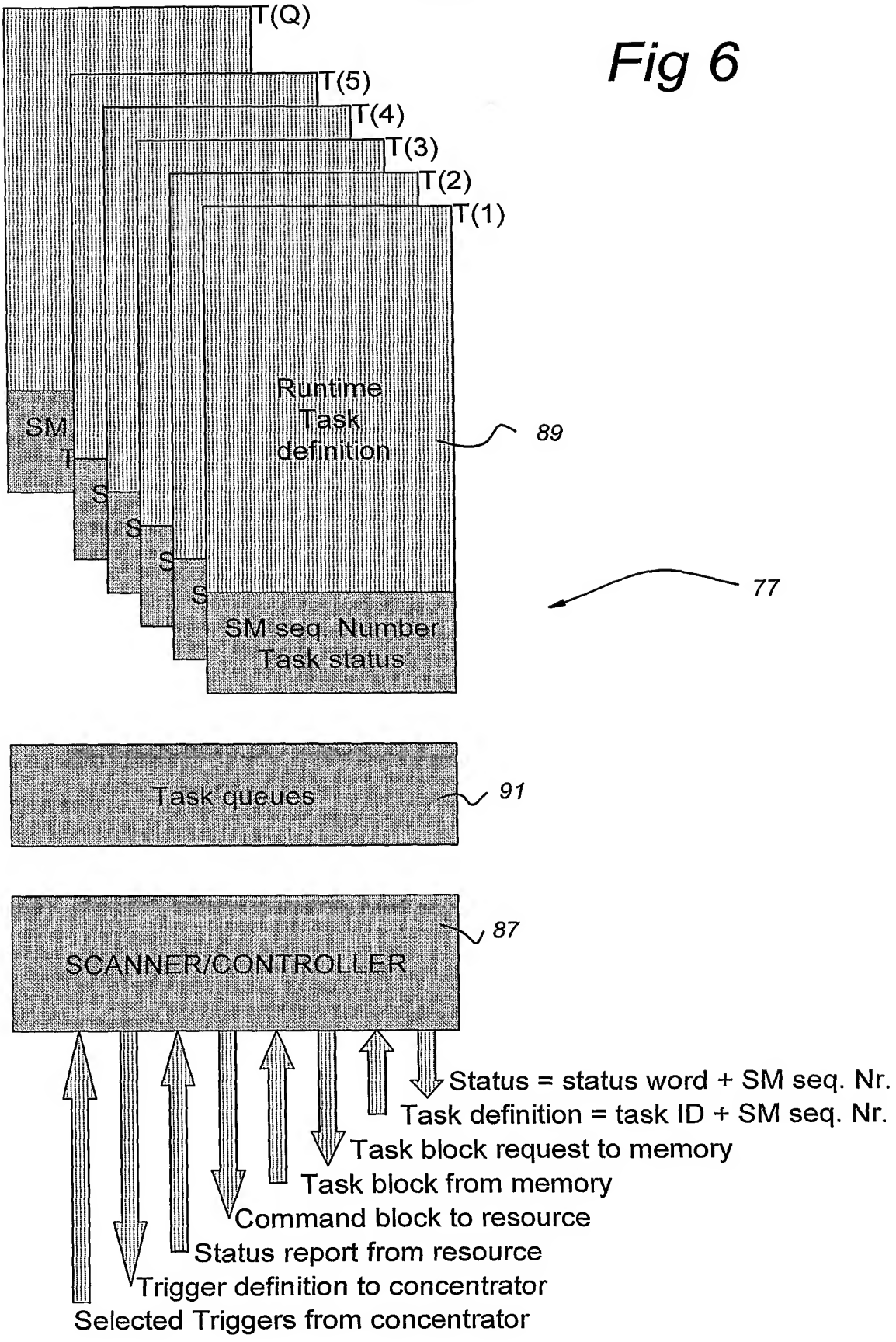

T(Q)
T(5)
T(4)
T(3)
T(2)
T(1)
SM
T
S
S
S
S
Runtime
Task
definition
89
77
SM seq. Number
Task status
Task queues
91
SCANNER/CONTROLLER
87
Status = status word + SM seq. Nr.
Task definition = task ID + SM seq. Nr.
Task block request to memory
Task block from memory
Command block to resource
Status report from resource
Trigger definition to concentrator
Selected Triggers from concentrator

Fig 7

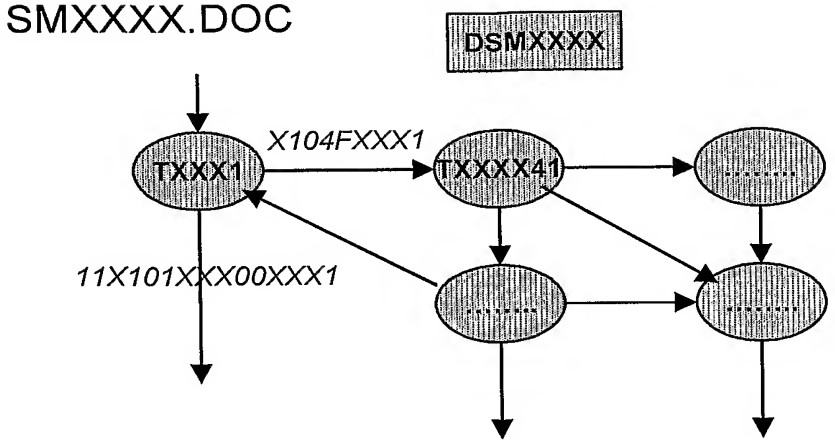
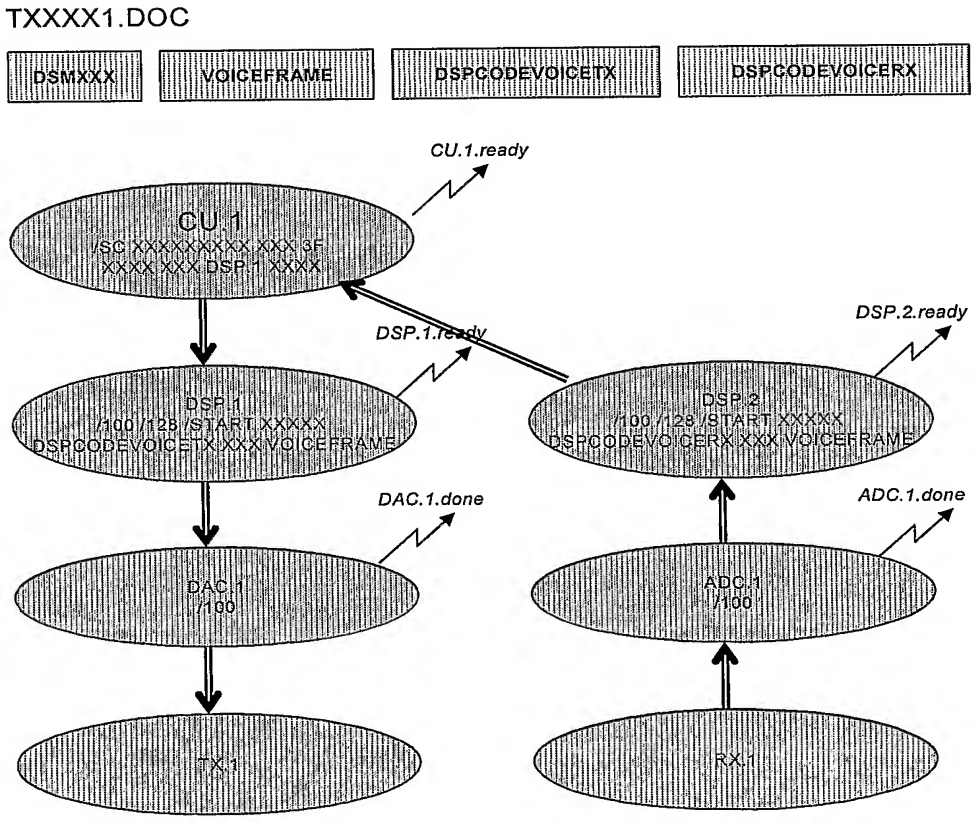


Fig 8



TASK-TRIGGERWORD:
1A,0,0,1,ADC.1.done,DAC.1.done,DSP.1.ready,DSP.2.ready,CU.1.ready,
DSP.1.status,DSP.2.status

Fig 9

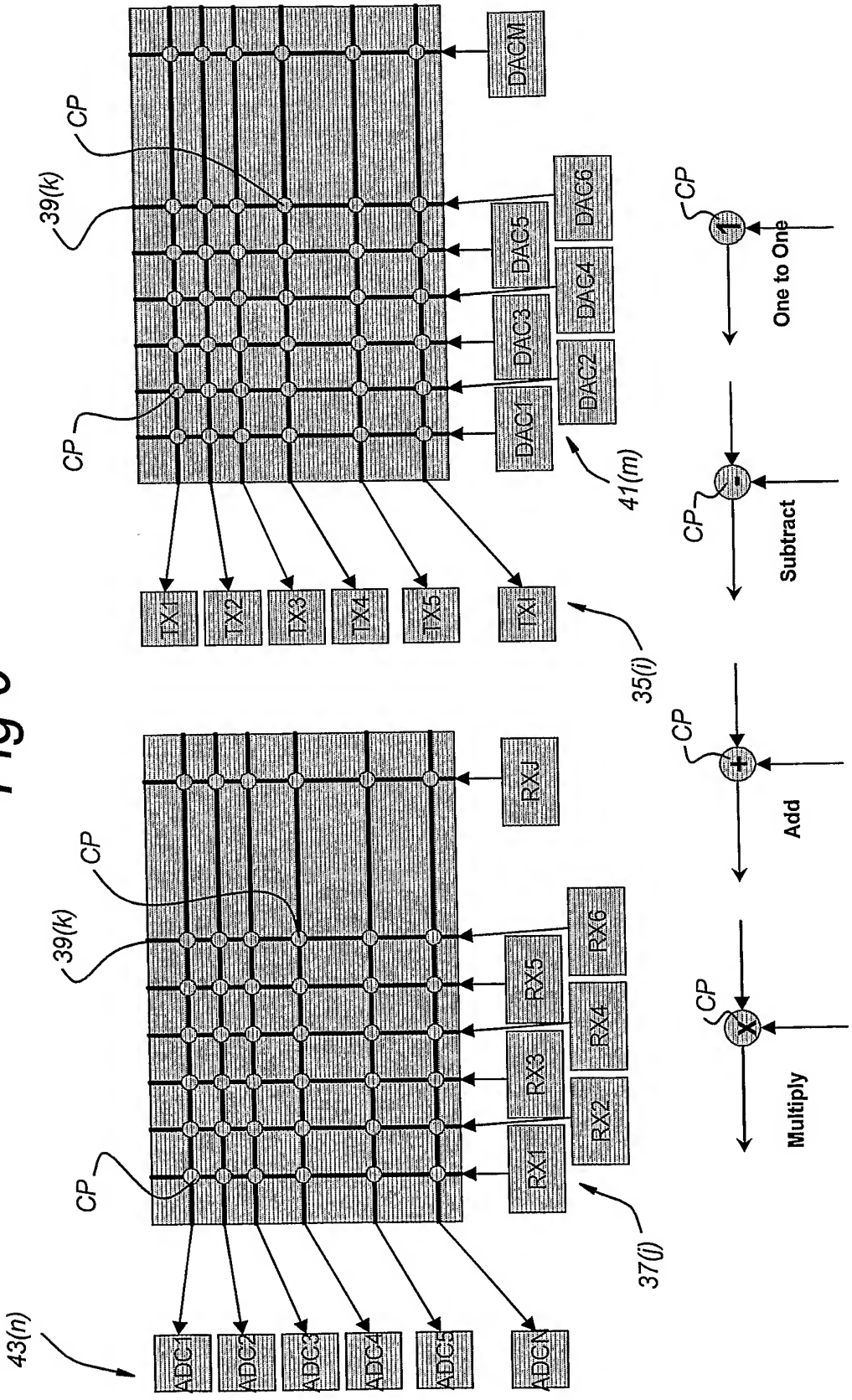

DACM
DAC6
DAC5
DAC4
DAC3
DAC2
DAC1
CP
39(k)
41(m)
TX1
TX2
TX3
TX4
TX5
TXI
35(i)
RXJ
RX6
RX5
RX4
RX3
RX2
RX1
37(j)
43(n)
ADC1
ADC2
ADC3
ADC4
ADC5
ADCN
One to One
Subtract
Add
Multiply

Fig 10

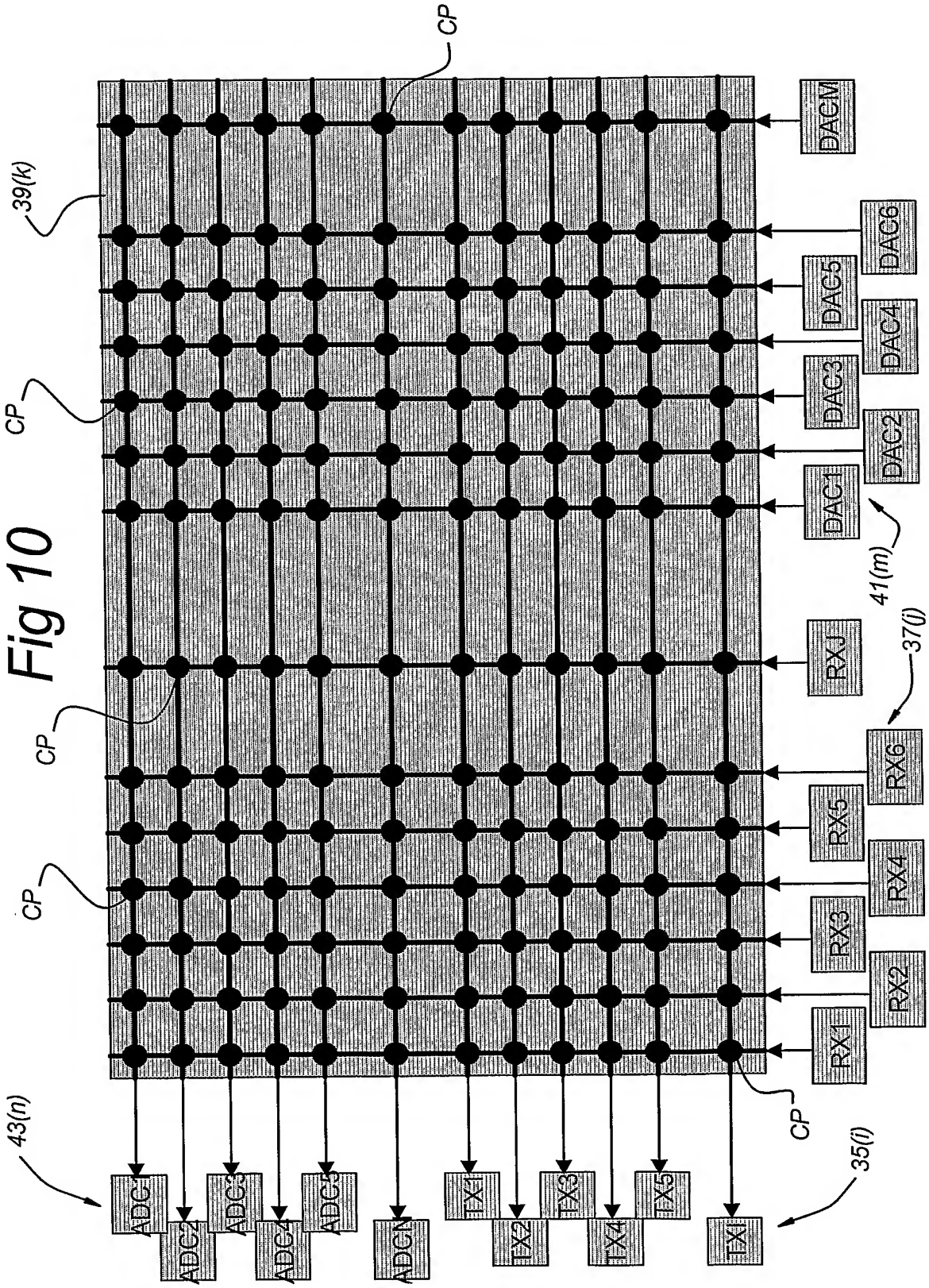

CP
39(k)
CP
CP
CP
CP
DACM
DAC6
DAC5
DAC4
DAC3
DAC2
DAC1
41(m)
RXJ
37(j)
RX6
RX5
RX4
RX3
RX2
RX1
43(n)
ADC1
ADC2
ADC3
ADC4
ADC5
ADCN
TX1
TX2
TX3
TX4
TX5
TXI
35(i)

Fig 11

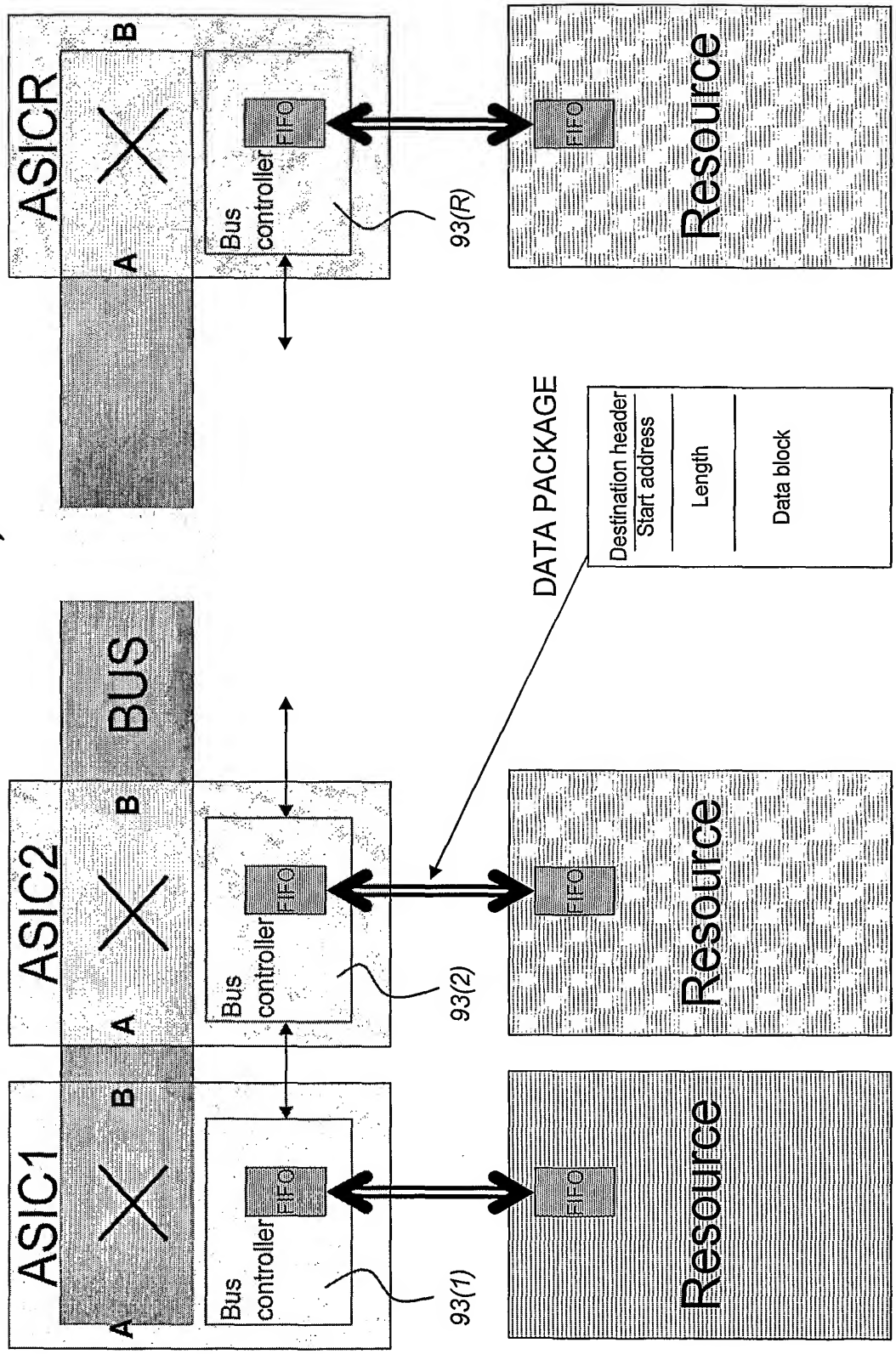

51
ASICR
A
B
Bus controller
FIFO
93(R)
Resource
ASIC2
93(2)
ASIC1
93(1)
BUS
DATA PACKAGE
Destination header
Start address
Length
Data block

Fig 12

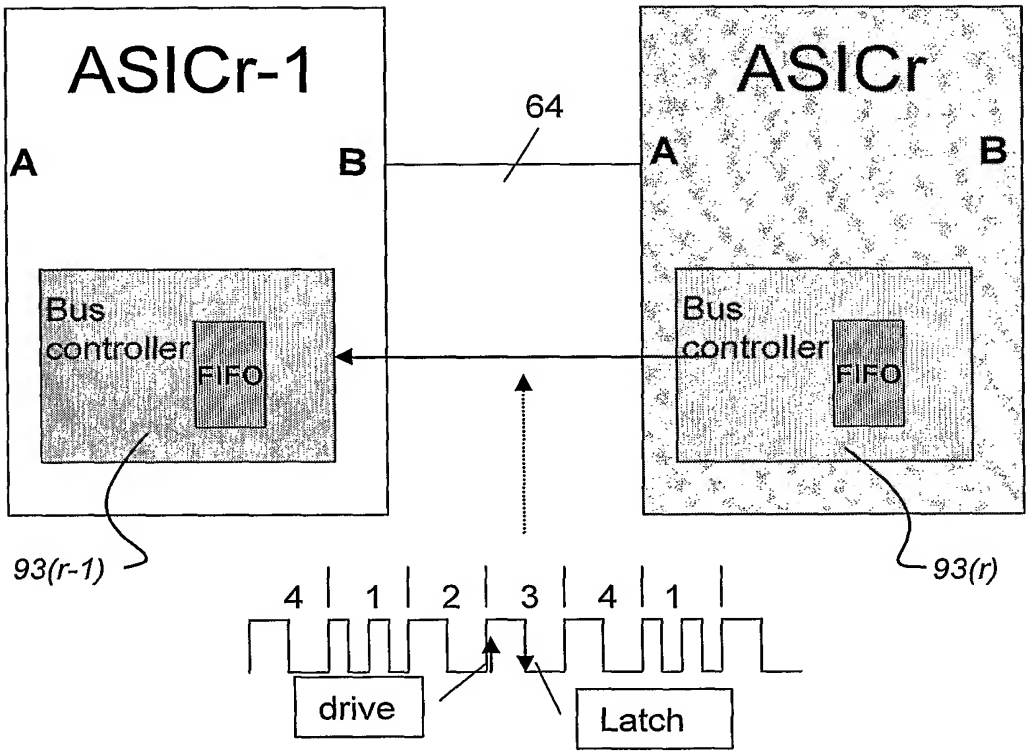

ASICr-1
A
B
Bus controller
FIFO
93(r-1)
64
ASICr
A
B
Bus controller
FIFO
93(r)
4
1
2
3
4
1
drive
Latch

Fig 13

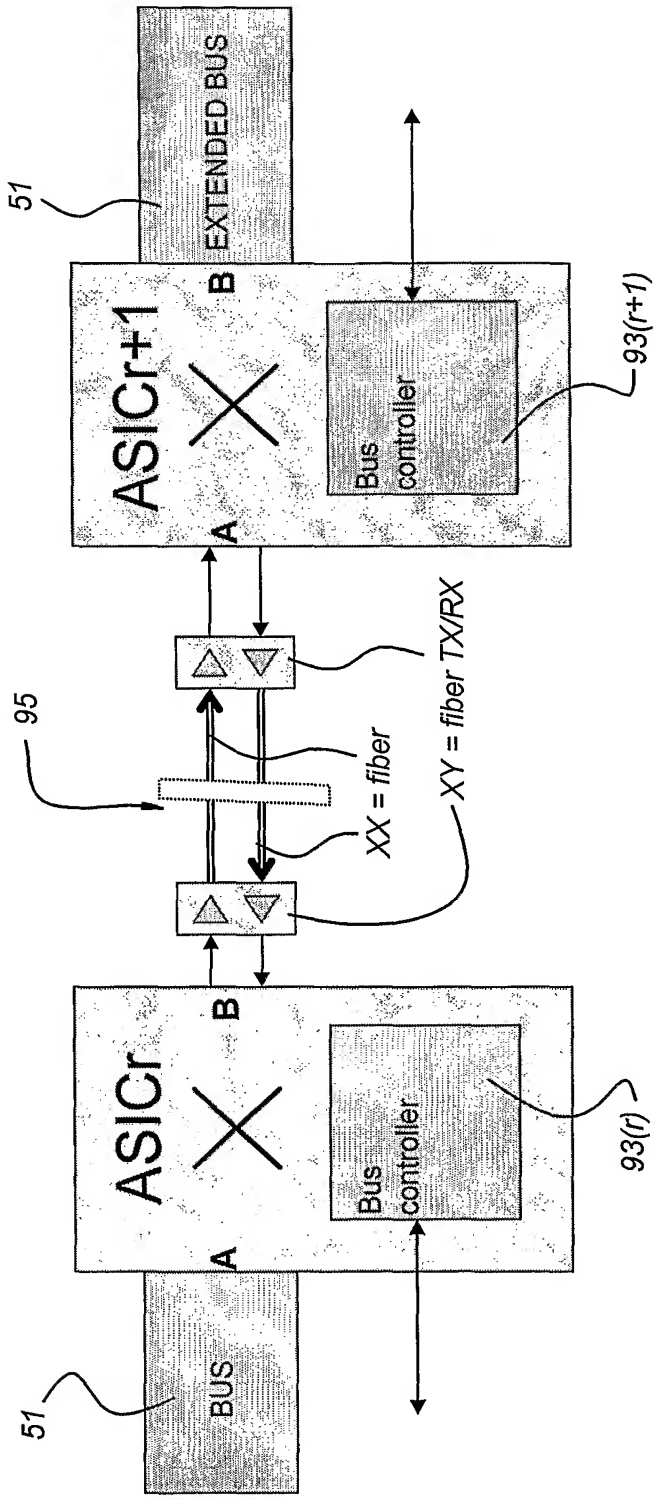

EXTENDED BUS
51
ASICr+1
B
A
Bus controller
93(r+1)
95
XX = fiber
XY = fiber TX/RX
ASICr
B
A
Bus controller
93(r)
BUS
51

Fig 14

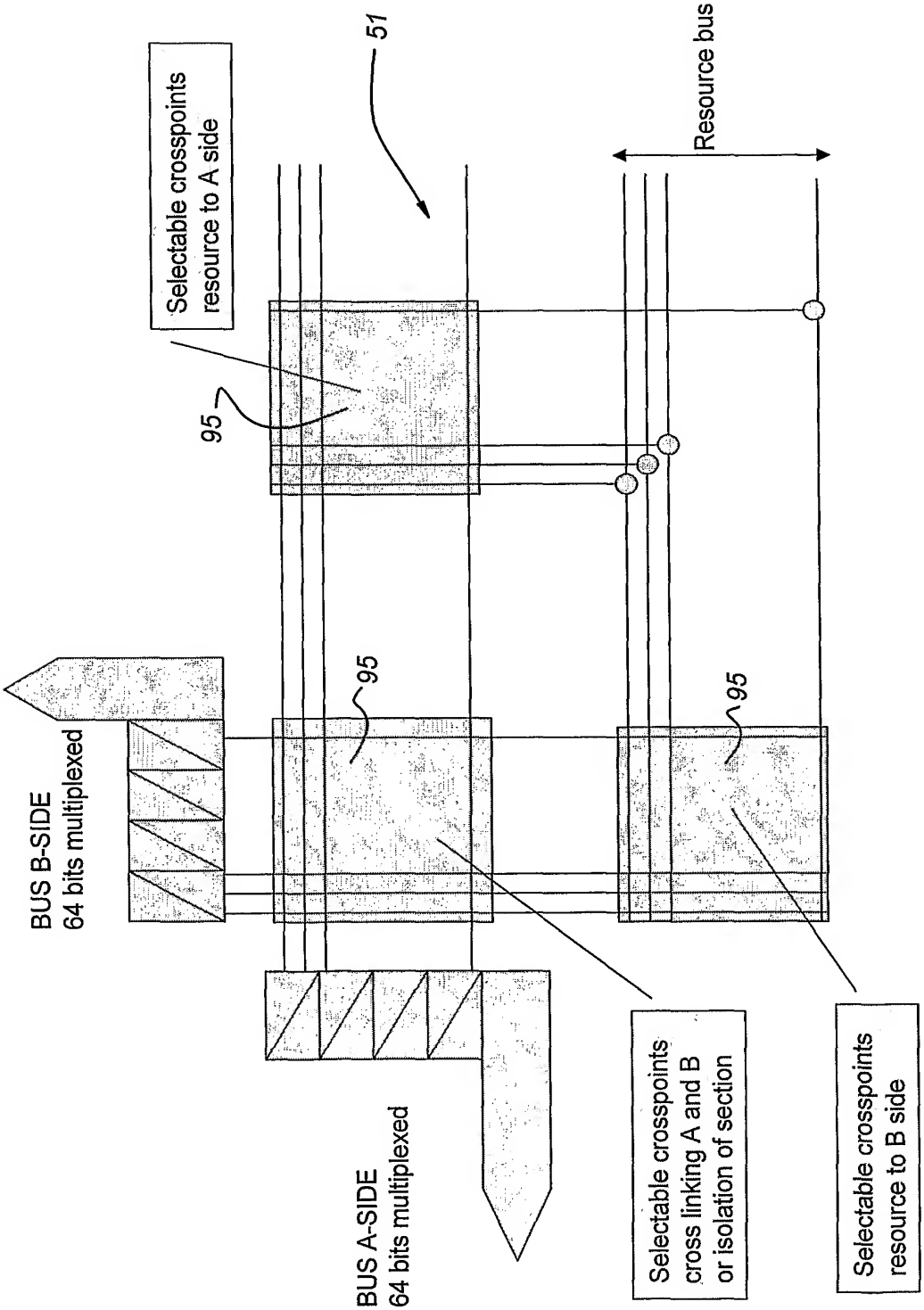

Selectable crosspoints resource to A side
51
Resource bus
95
95
95
BUS B-SIDE
64 bits multiplexed
BUS A-SIDE
64 bits multiplexed
Selectable crosspoints cross linking A and B or isolation of section
Selectable crosspoints resource to B side

Fig 15

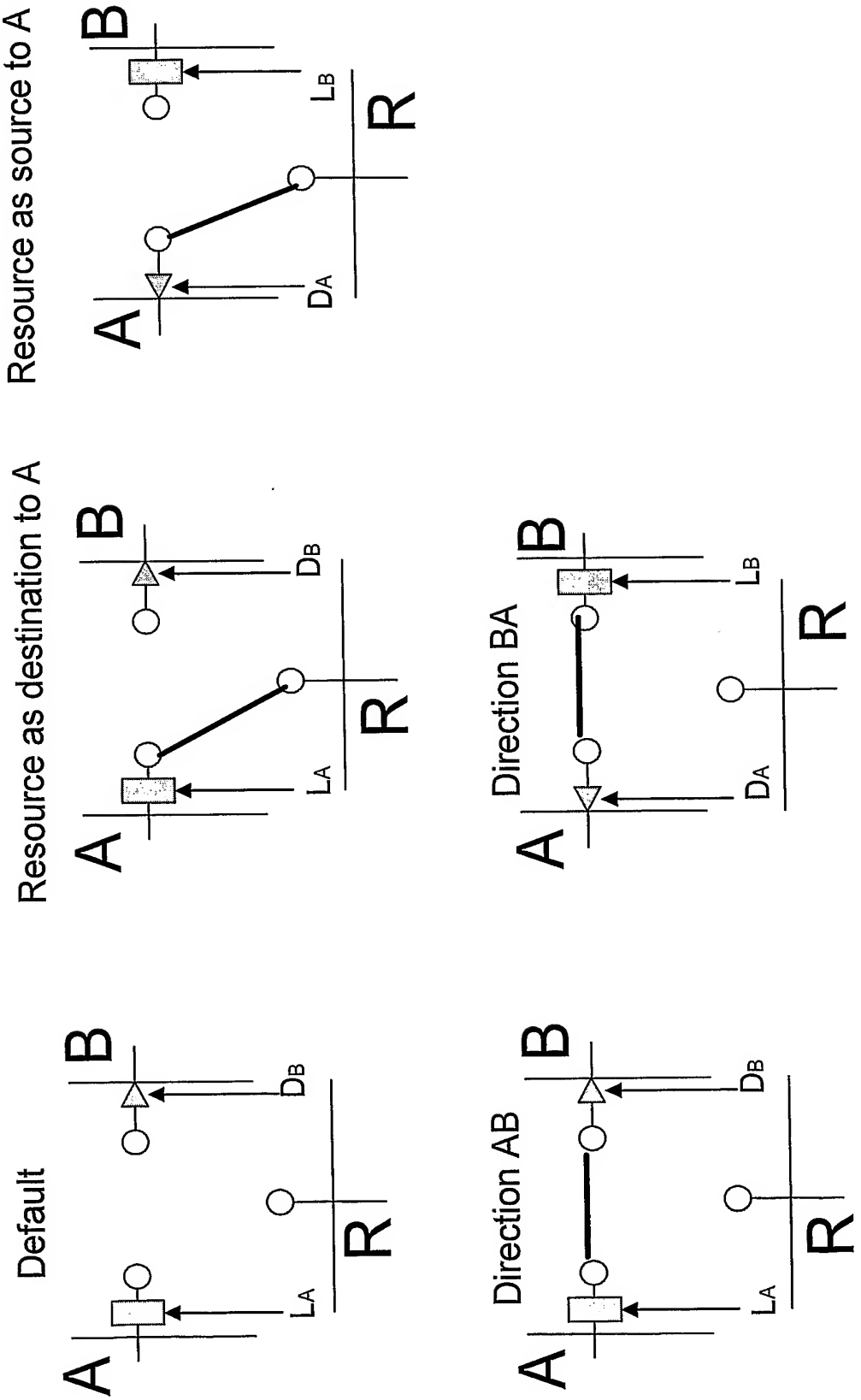

Default
A
B
R
L_A
D_B
Resource as destination to A
A
B
R
L_A
D_B
Resource as source to A
A
B
R
D_A
L_B
Direction AB
A
B
R
L_A
D_B
Direction BA
A
B
R
D_A
L_B

Fig 16a

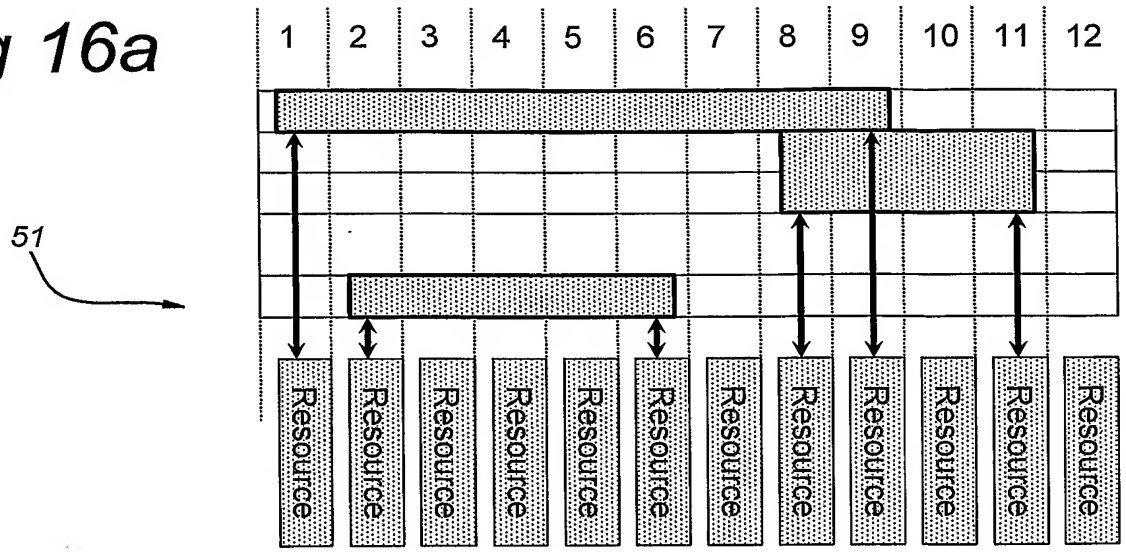


Fig 16b

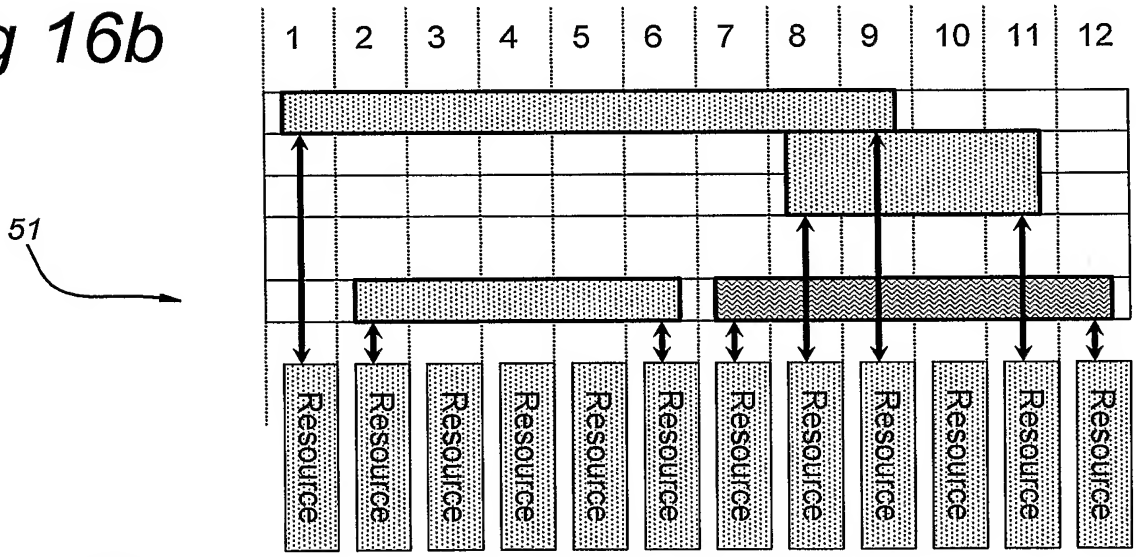


Fig 16c

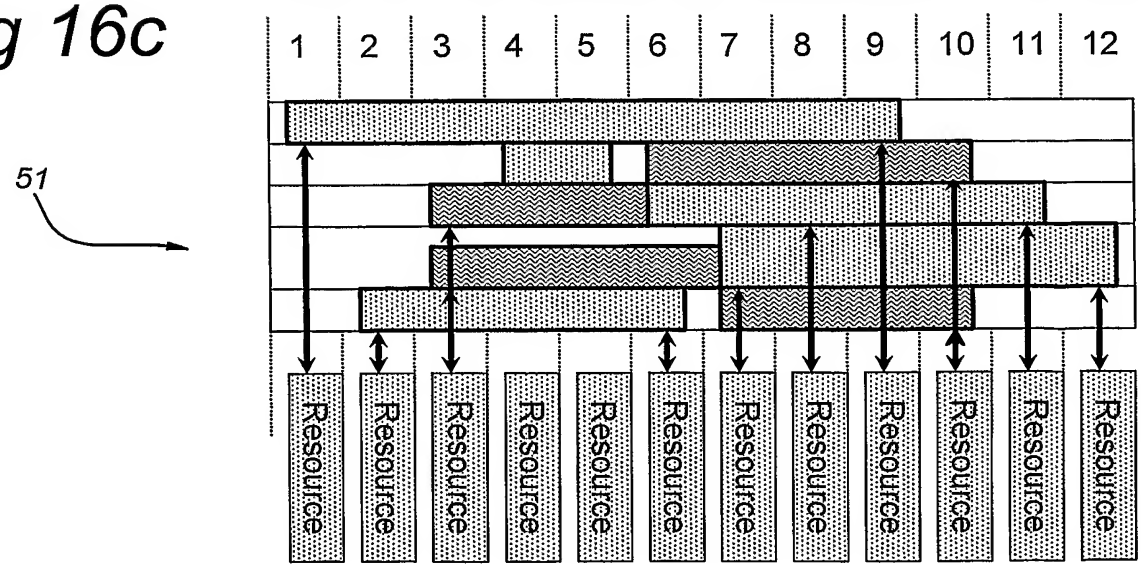
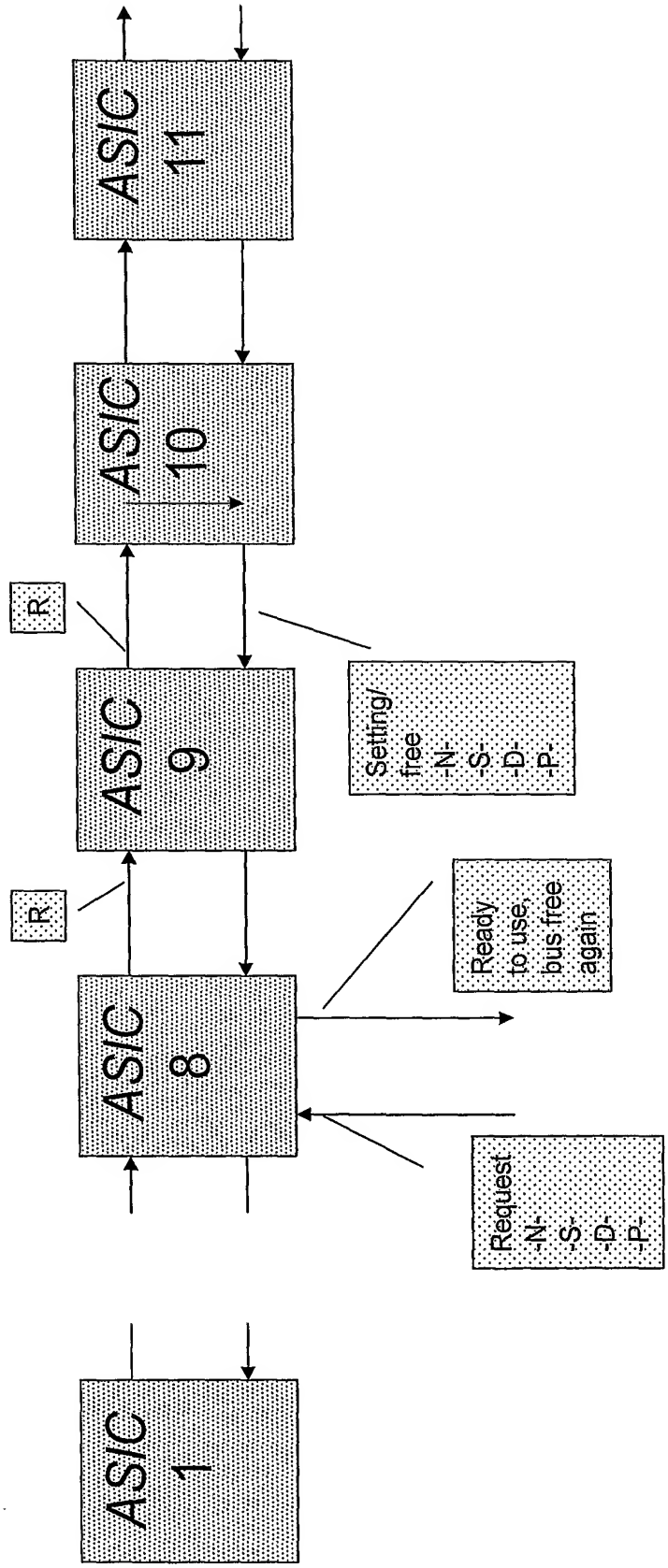


Fig 17


ASIC 11
ASIC 10
R
ASIC 9
Setting/ free -N- -S- -D- -P-
R
Ready to use, bus free again
ASIC 8
Request -N- -S- -D- -P-
ASIC 1